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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,474	06/25/2001	Matthew J. Amatangelo	AUS920010049US1	8686

35236 7590 09/16/2005

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,474	AMATANGELO ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-18 of U.S. Application 09/888,474, originally filed on 6/25/2001, are presented for examination.
2. Applicants' arguments dated 7/6/05 have been found to be unpersuasive. This action is final.

Claim Interpretations

3. Examiner interprets the term "timing element" according to the following section of the specification (See PG Pub No. 2003/0009318 A1, col.2, paragraph 11; and col.3, paragraph 32):

> The term "timing element" refers to an element according to the invention which represents the timing characteristics of a timing determinant block or a portion of such block. (col.2, para.11)
>
> The present invention utilizes a number of basic timing elements which are pieced together to represent the timing in a circuit, particularly a circuit which may be difficult for a static timing analysis tool to analyze. The types of timing elements used according to the invention will depend upon the circuitry to be modeled. At the very least, a timing element must be available to represent the propagation delay within the circuitry to be modeled. Such a delay timing element will be described below with reference to Figs.1 and 2. (col.3, para. 32)

4. Examiner interprets "timing element set" as referring to a collection of such "timing elements".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The prior art used for these rejections is as follows:

7. Avidan, J. U.S. Patent No. 6,158,022. Issued Dec.5, 2000. (Henceforth referred to as "**Avidan**").

8. The claim rejections are hereby summarized for Applicants' convenience. The detailed rejections follow.

9. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Avidan.

10. In regards to Claim 1, Avidan teaches the following limitations:

1. A method for analyzing an electronic circuit, the method comprising steps of:

(a) replacing at least one timing determinant block in a first functional component of the circuit with a timing element set;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the

first functional component; and
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(d) performing a static timing analysis for the circuit utilizing the timing model for the first functional component.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

Examiner notes that Avidan expressly teaches the creation of a "grey box model" of the circuit under analysis (See col.15, lines 35-39):

> The present invention will generate a grey box model for the circuit under analysis if the user so directs. Alternatively, the user may compile a gray box model manually. Programmatic generation of the gray box model occurs in conjunction with the circuit analysis described above.

Examiner also notes that not only is Item 1500 in Fig.15A of the instant application is a Gray Box Model, but also that the instant application recites (see PG Pub, col.7, para.65. Emphasis added):

> The process also preferably includes formatting the resulting ***gray box models produced according to the invention.*** This formatting step is shown at step 1612 in Fig.16, and is required in order to place the model information in a form usable by the particular static timing analysis tool to be used in performing the static timing analysis. The invention also preferably includes storing these gray box models, preferably in formatted form, in a gray box library for use by a static timing analysis tool as described below.

Examiner therefore finds that the Gray Box Models taught and claimed in Avidan correspond to the Gray Box Models taught and claimed in the instant application.

11. In regards to Claim 2, Avidan teaches the following limitations:

2. The method of Claim 1 further comprising the step of:
(a) identifying an additional functional component from the circuit to be analyzed.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

In particular, Col.5, lines 62-64 of Avidan teach (emphasis added):

> The present invention calculates the delay for ***each stage in a path***, and the total delay of the path is the sum of the delays along the path.

In addition, Col.6, lines 5-8 of Avidan teach (emphasis added):

> The present invention calculates the delay ***for each stage*** by the EPIC Piecewise Linear Model available from the assignee of this patent application.

Examiner notes that the instant application recites that:

> The actual static timing analysis step is shown at process block 1614 in Fig.16. This step may be performed in any suitable fashion and is preferably performed with a static timing analysis tool such as the PATHMILL software product by EPIC Design Technology.

12. In regards to Claim 3, Avidan teaches the following limitations:

3. The method of Claim 2 further comprising the steps of:

(a) replacing at least one timing determinant block in the additional functional component with an additional timing element set;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(b) performing a circuit simulation for a cross-section of the additional functional component to determine the timing characteristics associated with each replaced timing determinant block of the additional functional component;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(c) attaching the timing characteristics associated with each replaced timing determinant block of the additional functional component to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the additional functional component; and
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(d) wherein the step of performing a static timing analysis for the circuit also utilizes the timing model for the additional functional component.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

13. In regards to Claim 4, Avidan teaches the following limitations:

4. The method of Claim 1 further including the step of :

(a) selecting the cross-section of the first functional component to produce a worst-case timing path through the functional component.
(Avidan, especially: col.15, lines 34 to 63)

14. In regards to Claim 5, Avidan teaches the following limitations:

5. The method of Claim 1 further including the step of:

(a) selecting the cross-section of the first functional component to produce a best-case timing path through the functional component.
(Avidan, especially: col.15, lines 34 to 63)

15. In regards to Claim 6, Avidan teaches the following limitations:

6. The method of Claim 1 further including the step of:

(a) developing a group of timing elements for use in producing timing element sets suitable for replacing a number of different timing determinant blocks .
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

16. In regards to Claim 7, Avidan teaches the following limitations:

7. The method of Claim 1 wherein each timing determinant block in the first functional component is replaced with a respective tuning element set.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

17. In regards to Claim 8, Avidan teaches the following limitations:

8. A method of producing a timing model for use in static timing analysis for an electronic circuit, the method comprising the steps of :

(a) replacing at least one timing determinant block in a functional component of the circuit with a timing element set;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(b) performing a circuit simulation for a cross-section of the functional component to determine timing characteristics associated with each replaced timing determinant block of the functional component; and
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective tuning determinant block.

(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

Examiner notes that Avidan expressly teaches the creation of a "grey box model" of the circuit under analysis (See col.15, lines 35-39):

> The present invention will generate a grey box model for the circuit under analysis if the user so directs. Alternatively, the user may compile a gray box model manually. Programmatic generation of the gray box model occurs in conjunction with the circuit analysis described above.

Examiner also notes that not only is Item 1500 in Fig.15A of the instant application is a Gray Box Model, but also that the instant application recites (see PG Pub, col.7, para.65. Emphasis added):

> The process also preferably includes formatting the resulting ***gray box models produced according to the invention.*** This formatting step is shown at step 1612 in Fig.16, and is required in order to place the model information in a form usable by the particular static timing analysis tool to be used in performing the static timing analysis. The invention also preferably includes storing these gray box models, preferably in formatted form, in a gray box library for use by a static timing analysis tool as described below.

Examiner therefore finds that the Gray Box Models taught and claimed in Avidan correspond to the Gray Box Models taught and claimed in the instant application.

18. In regards to Claim 9, Avidan teaches the following limitations:

9. The method of Claim 8 further including the step of :
(a) selecting the cross-section of the functional component to produce a worst-case timing path through the functional component.
(Avidan, especially: col.15, lines 34 to 63)

19. In regards to Claim 10, Avidan teaches the following limitations:

10. The method of Claim 8 further including the step of:
(a) selecting the cross-section Of the first functional component to produce a best-case timing path through the functional component.
(Avidan, especially: col.15, lines 34 to 63)

20. In regards to Claim 11, Avidan teaches the following limitations:

11. The method of Claim 8 further including the step of :
(a) developing a group of timing elements for use in producing timing element sets suitable for replacing a number of different timing determinant blocks.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

21. In regards to Claim 12, Avidan teaches the following limitations:

12. The method of Claim 8 wherein each timing determinant block in the functional component is replaced with a respective timing element set.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

22. In regards to Claim 13, Avidan teaches the following limitations:

13. The method of Claim 8 wherein the cross-section for the circuit simulation is selected to provide information on a first signal path through the functional component and further including the step of performing a second circuit simulation for a different cross-section of the functional component to determine timing characteristics associated with each replaced timing determinant block of the functional component for that different cross-section.
(Avidan, especially: col.15, line 50 to col.16, line 4)

23. In regards to Claim 14, Avidan teaches the following limitations:

14. A method for employing timing elements to create a timing model for a functional component of a circuit, the method comprising the steps of:

(a) defining a group of timing elements, each timing element in the group comprising an element for representing at least a portion of the timing characteristics associated with a timing determinant block within the functional component;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(b) replacing at least one timing determinant block in the functional component with a timing element set including one or more of the timing elements from the group of timing elements;
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(c) performing a circuit simulation for a cross-section of the functional component to determine simulated timing characteristics associated with each replaced timing determinant block of the functional component; and
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

(d) attaching the simulated timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block.
(Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

Examiner notes that Avidan expressly teaches the creation of a "grey box model" of the circuit under analysis (See col.15, lines 35-39):

> The present invention will generate a grey box model for the circuit under analysis if the user so directs. Alternatively, the user may compile a gray box model manually. Programmatic generation of the gray box model occurs in conjunction with the circuit analysis described above.

Examiner also notes that Item 1500 in Fig.15A of the instant application is a Gray Box Model, and also that the instant application recites (see PG Pub, col.7, para.65. Emphasis added):

> The process also preferably includes formatting the resulting ***gray box models produced according to the invention.*** This formatting step is shown at step 1612 in Fig.16, and is required in order to place the model information in a form usable by the particular static timing analysis tool to be used in performing the static timing analysis. The invention also preferably includes storing these gray box models, preferably in formatted form, in a gray box library for use by a static timing analysis tool as described below.

Examiner therefore finds that the Gray Box Models taught and claimed in Avidan correspond to the Gray Box Models taught and claimed in the instant application.

24. In regards to Claim 15, Avidan teaches the following limitations:

15. The method of Claim 14 further including the step of:
(a) selecting the cross-section of the functional component to produce a worst-case timing path through the functional component.
(Avidan, especially: col.15, lines 34 to 63)

25. In regards to Claim 16, Avidan teaches the following limitations:

16. The method of Claim 14 further including the step of:
(a) selecting the cross-section of the first functional component to produce a best-case timing path through the functional component.

(Avidan, especially: col.15, lines 34 to 63)

26. In regards to Claim 17, Avidan teaches the following limitations:

> 17. The method of Claim 14 wherein each timing determinant block in the functional component is replaced with a respective timing element set.
> (Avidan, especially: col.2, line 55 to col.3, line 27; and col.5, line 60 to col.6, line 12)

27. In regards to Claim 18, Avidan teaches the following limitations:

> 18. The method of Claim 14 wherein the cross-section for the circuit simulation is selected to provide information on a first signal path through the functional component and further including the step of performing a second circuit simulation for a different cross-section of the functional component to determine simulated timing characteristics associated with each replaced timing determinant block of the functional component for that different cross-section.
> (Avidan, especially: col.15, line 50 to col.16, line 4)

Response to Arguments

Re: The Foltin Reference

28. In their response (see pp.2-3 of the arguments filed on 7/6/2005), the applicants objected to Examiner's citation of the Foltin reference in the text of the original 35 U.S.C. §102 rejection based on the Avidan reference. The cited section of the Foltin reference in the original rejection merely summarized the teachings of the Avidan reference, in particular that Avidan teaches the creation of a grey box model. Since Avidan expressly teaches the creation of a grey box model (see col.15, lines 35-39), the Foltin reference was unnecessary. While this form of multiple-reference 35 U.S.C. §102 rejection is proper (see MPEP §2131.01 for details), Examiner has decided to delete all references to Foltin from the 35 U.S.C. §102 rejections in order to simplify the record.

29. Examiner previously pointed out to Applicants' Representative that Avidan expressly teaches "grey box models" in the Interview Summary dated 4/27/2005 (see paragraph 4 of the Interview Summary).

Re: The Avidan Reference

30. In their response (see p.4 of the arguments filed on 7/6/2005), the applicants unpersuasively presented the following arguments regarding the Avidan reference:

    a. Avidan "fails to teach" the limitations of element (b) of claim 1,

    > (b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;

    b. Avidan "fails to teach" the limitations of element (d) of claim 1,

    > (d) performing a static timing analysis for the circuit utilizing the timing model for the first functional component.

    c. Applicants' "grey box" differs from Avidan's "grey box".

31. Examiner notes that according to MPEP § 2131:

> The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

32. Examiner respectfully disagrees to Applicants' first argument, that Avidan does not teach element (b) of claim 1:

> (b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;

For example, Avidan teaches (See Avidan: col.6, lines 5-9. Emphasis added):

> The present invention calculates the delay for **each stage** by running a transient analysis on the stage, with transistors being modeled by the EPIC Piecewise Linear Model available from the assignee of this patent application.

Avidan also teaches (See Avidan: col.15, line 35 to col.16, line 3):

> The present invention determines the delay from a primary clock to a clock pin of a sequential element only at the end of the analysis while producing the gray box block model as output.
>
> The process of collecting data for the gray box model is very efficient since the present invention processes only the paths between two sequential elements which contain purely combinatorial gates. When generating a gray box block model, the present invention does not process paths which go through a sequential element requiring transparency.
>
> **For each processed path, the present invention saves the maximum and minimum delays as well as the delays for the different logic conditions (i.e., a rising and a falling signal) on the first and last node of the path.**
>
> **The worst and best case data the present invention stores if there are multiple paths between the start and end points.** In a preferred embodiment, the present invention hashes data to be stored in order to achieve faster access.
>
> At the end of the circuit analysis, the present invention produces the gray box model data. In addition to this gray box data, the present invention writes setup and hold times for each primary input. This additional data provides the ability to switch between gray box and black box blocks at the full chip level without the need to generate or regenerate the corresponding black box model.

33. Examiner respectfully disagrees to Applicants' second argument, that Avidan does not teach element (d) of claim 1:

> (d) performing a static timing analysis for the circuit utilizing the timing model for the first functional component.

For example, Avidan teaches (See Avidan: col.1, lines 23-42. Emphasis added):

> This invention relates to circuit analyzers. In particular, this invention

relates to circuit analyzers performing **static analysis** of circuits including black box timing models.

Circuit analyzers in the art fall into one of two general categories: dynamic and static. With dynamic analyzers, the design or diagnostic engineer must provide sets of waveforms to simulate the conditions under which a circuit will operate. Of course, the more the sets reflect all possible operating conditions, the more accurate the result of the dynamic analysis can be. The cost, however, of producing exhaustive waveform sets can be extremely high.

Static analyzers, on the other hand, relieve the design engineer of the trouble of supplying comprehensive input vectors. A **static analyzer** can identify critical paths in a circuit, find timing errors and estimate overall performance. This waveform independence is particularly efficient and useful for large systems. Such **static analyzers** can identify critical paths which the test patterns do not exercise during timing simulation.

34. Examiner respectfully disagrees to Applicants' third argument, that Applicants' "grey box" differs from Avidan's "grey box" because "Avidan fails to disclose performing a circuit simulation to determine timing characteristics." Examiner finds that the above cited section of Avidan (col.15, line 35 to col.16, line 3) refutes this argument.

Conclusion

35. Applicants' arguments filed 7/6/2005 have been fully considered but they are not persuasive.

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

September 12, 2005

Paul L. Rodriguez 9/14/05

Primary Examiner
Art Unit 2125